AMENDMENTS

LISTING OF CLAIMS:

1. (Currently amended) An interleave control device using a nonvolatile ferroelectric memory, comprising:

a single chip FeRAM array comprising a plurality of single banks, the single chip FeRAM array controls ~~which controls~~ access time differently in each address ~~and includes a plurality of single banks~~;

a memory interleave controller including:

a nonvolatile interleave program register, including a program register array, configured to program a code for controlling the interleave using a nonvolatile ferroelectric memory; and

an interleave controller configured to output a control signal for changing an address path of the signal chip FeRAM array depending on the programmed code by the nonvolatile interleave program register,

wherein the nonvolatile ferroelectric memory ~~configured program~~ programs a code for differently controlling a memory interleave operation depending on an access latency time and a restore latency time which are set in a memory interleave region corresponding to lower address bits of row address bits ~~in a nonvolatile ferroelectric memory, and to change an address path of the single chip FeRAM array depending on the code programmed in the nonvolatile ferroelectric memeory~~; and

a bus configured to transfer data between the single chip FeRAM array and the memory interleave controller.

2. (Cancelled)

3. (Currently amended) The device according to claim 1, wherein ~~An interleave control device using a nonvolatile ferroelectric memory, comprising:~~

~~a single chip FeRAM array which controls access time differently in each address and includes a plurality of single banks;~~

~~a memory interleave controller configured to program a code for differently controlling a memory interleave operation depending on kind of the address in a nonvolatile ferroelectric memory, and to change an address path of the single chip FeRAM array depending on the code programmed in the nonvolatile ferroelectric memory, the memory interleave controller including:~~

~~the nonvolatile interleave program register configured to program a code for controlling the interleave using a nonvolatile ferroelectric memory,~~ the nonvolatile interleave program register ~~includes~~ comprises:

a program command processor configured to output a command signal for coding a program command in response to a write enable signal, a chip enable signal, an output enable signal and a reset signal;

a program register controller configured to logically operate the command signal, input data and a power-up detecting signal, and to output a write control signal and a cell plate signal; and

[[a]] the program register array, including a nonvolatile ferroelectric memory device, configured to output a programmed code signal in response to the write control signal, the cell plate signal, a pull-up enable signal and a pull-down enable signal ~~and~~

~~an interleave controller configured to output a control signal for changing an address path of the signal chip FeRAM array depending on the programmed code by the nonvolatile interleave program register; and~~

~~a bus configured to transfer data between the single chip FeRAM array and the memory interleave controller~~.

4. **(Original)** The device according to claim 3, wherein the nonvolatile interleave program register further comprises a reset circuit unit configured to output the reset signal into the program register controller in a power-up mode.

5. **(Original)** The device according to claim 3, wherein the program command processor comprises:

a logic unit configured to logically operate the write enable signal, the chip enable signal, the output enable signal and the reset signal;

a flip-flop unit configured to sequentially flip-flop toggles of the output enable signal in response to an output signal from the logic unit, and to output the command signal; and

an over-toggle detector configured to detect over-toggles of the output enable signal.

6. **(Original)** The device according to claim 5, wherein the logic unit comprises:

a first NOR gate configured to perform a NOR operation on the write enable signal and the chip enable signal;

a first AND gate configured to perform an AND operation on an output signal from the first NOR gate and the output enable signal; and

a second AND gate configured to perform an AND operation on an output signal from the first NOR gate, an inverted reset signal and an output signal from the over-toggle detector.

7. **(Original)** The device according to claim 5, wherein the over-toggle detector comprises a third NAND gate configured to perform a NAND operation on the command signal and the output enable signal.

8. **(Original)** The device according to claim 3, wherein the program register controller comprises:

a third AND gate configured to perform an AND operation on the command signal and the input data;

a first delay unit configured to non-invert and delay an output signal from the third AND gate;

a second NOR gate configured to perform a NOR operation on output signals from the third AND gate and from the first delay unit;

a second delay unit configured to delay an output signal from the second NOR gate, and to output the write control signal;

a third NOR gate configured to perform a NOR operation on an output signal from the second NOR gate and the power-up detecting signal; and

a third delay unit configured to invert and delay an output signal from the third NOR gate, and to output the cell plate signal.

9. **(Original)** The device according to claim 3, wherein the program register array comprises:

a pull-up driver configured to pull up a power voltage when the pull-up enable signal is enabled;

a first driving unit configured to be cross-coupled to both ends of a program register, and to driver a voltage applied from the pull-up driver;

a write enable controller configured to output the reset signal and a set signal into both ends of the program register in response to the write control signal;

a ferroelectric capacitor configured to generate voltage difference between both ends of the program register in response to the cell plate signal;

a pull-down driver configured to pull down a ground voltage when the pull-down enable signal is enabled; and

a second driving unit configured to be cross-coupled to both ends of the program register, and to drive a voltage applied from the pull-down driver.

Claims 10-20 canceled.